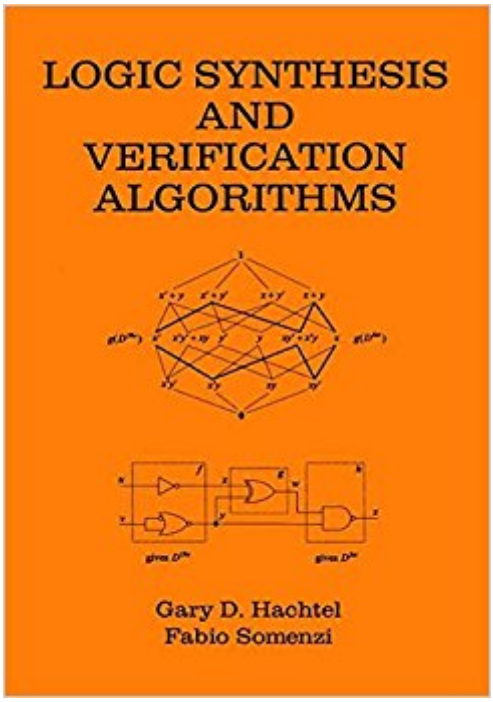
Logic Synthesis And Verification Algorithms



Synopsis

Logic Synthesis and Verification Algorithms is a textbook designed for courses on VLSI Logic Synthesis and Verification, Design Automation, CAD and advanced level discrete mathematics. It also serves as a basic reference work in design automation for both professionals and students. Logic Synthesis and Verification Algorithms is about the theoretical underpinnings of VLSI (Very Large Scale Integrated Circuits). It combines and integrates modern developments in logic synthesis and formal verification with the more traditional matter of Switching and Finite Automata Theory. The book also provides background material on Boolean algebra and discrete mathematics. A unique feature of this text is the large collection of solved problems. Throughout the text the algorithms covered are the subject of one or more problems based on the use of available synthesis programs.

Book Information

Hardcover: 564 pages

Publisher: Springer; 1996 edition (June 30, 1996)

Language: English

ISBN-10: 0792397460

ISBN-13: 978-0792397465

Product Dimensions: 1 x 7 x 10 inches

Shipping Weight: 3.4 pounds (View shipping rates and policies)

Average Customer Review: 4.2 out of 5 stars 4 customer reviews

Best Sellers Rank: #2,200,878 in Books (See Top 100 in Books) #81 inÂ Books > Engineering & Transportation > Engineering > Electrical & Electronics > Circuits > VLSI & ULSI #370 inÂ Books > Computers & Technology > Programming > Software Design, Testing & Engineering > Logic #646 inÂ Books > Engineering & Transportation > Engineering > Electrical & Electronics > Circuits > Design

Customer Reviews

In the last decade logic synthesis has gained widepsread acceptance by designers.Â Formal verification is now advancing along the same path.Â Computer aided design tools for logic synthesis and verification have become the primary instrument for coping with the ever increasing complexity of designs, and ever more stringent time-to-market constraints.Â Effective design must be based on thorough understanding of the capabilities, limitations, and algorithmic principles employed by these tools.Â In this book we provide a foundation for such understanding. Logic

Synthesis and Verification Algorithms blends mathematical foundations and algorithmic developments with circuit design issues.Â Each new technique is presented in the context of its application to design.Â Through the study of optimal two-level and multilevel combinational circuit design, the reader is introduced to basic concepts, such as Boolean algebras, local search, and algebraic factorization. Similarly, through the study of optimal sequential circuit design, the reader is introduced to graph algorithms, finite state systems, and language theory.Â Throughout the book, recurrent themes such as branch and bound, dynamic programming, and symbolic implicit enumeration are used to establish optimal design principles. Circuit designers and CAD tool developers alike will find Logic Synthesis and Verification Algorithms useful as an introductory and reference text.Â The rich collection of examples and solved problems make this book ideal for self study. Because of its careful balance of theory and application, Logic Synthesis and Verification Algorithms will serve well as a textbook for upper division and first year graduate students in electrical and computer engineering. --This text refers to the Digital edition.

This is a very readable book that includes many helpful examples and exercises.Hachtel’s exposition is rigorous andÂ Logic Synthesis and Verification Algorithmscrystal clear.

The book covers most of the fundamental aspects of logic synthesis and verification algorithms commonly implemented in the popular CAD tools. However, the book is poorly written and full of typos. One may constantly wonder what is going on until he reads the material like the 2nd or 3rd times and guess his way through. Sadly, there is rarely a better book in the CAD field, so even though the book is not very well written the material presented is still worth reading especially for any serious readers working in the field of logic synthesis.

I had the oppurtunity to study this book in my graduate study. I think it is a well-written book, which has a substantial coverage of the field of logic synthesis and verification. I would highly recommend this book to advanced readers and those who are mathematically inclined. The expertise of the authors is reflected in the content of the book, and this can be fully appreciated by the readers having the qualifications mentioned above.

This book is good. It covers all the fundamentals needed to learn two level and multi level logic synthesis and verification.It’s a good stepping stone for those readers wanting to delve more into the IEEE publications area later on in their careers when implementing new algorithms for logic

synthesis.

Logic Synthesis and Verification Algorithms Handbook of Reagents for Organic Synthesis: Reagents for Heteroarene Synthesis (Hdbk of Reagents for Organic Synthesis) Logic Minimization Algorithms for VLSI Synthesis (The Springer International Series in Engineering and Computer Science) Evolutionary Algorithms in Theory and Practice: Evolution Strategies, Evolutionary Programming, Genetic Algorithms Bundle of Algorithms in C++, Parts 1-5: Fundamentals, Data Structures, Sorting, Searching, and Graph Algorithms (3rd Edition) (Pts. 1-5) Practical Algorithms in Pediatric Hematology and Oncology: (Practical Algorithms in Pediatrics. Series Editor: Z. Hochberg) Practical Algorithms in Pediatric Nephrology: (Practical Algorithms in Pediatrics. Series Editor: Z. Hochberg) Practical Algorithms in Pediatric Gastroenterology: (Practical Algorithms in Pediatrics. Series Editor: Z. Hochberg) Practical Algorithms in Pediatric Endocrinology: (Practical Algorithms in Pediatrics. Series Editor: Z. Hochberg) Algorithms for Reinforcement Learning (Synthesis Lectures on Artificial Intelligence and Machine Learning) The Politics of Weapons Inspections: Assessing WMD Monitoring and Verification Regimes Verification and Validation in Scientific Computing Medical Device Software Verification, Validation and Compliance SystemVerilog for Verification: A Guide to Learning the Testbench Language Features Advanced Verification Techniques: A SystemC Based Approach for Successful Tapeout Analog-Mixed Signal Verification Advanced Organic Chemistry: Part B: Reaction and Synthesis: Reaction and Synthesis Pt. B Landmarking and Segmentation of 3D CT Images (Synthesis Lectures on Biomedical Engineering Synthesis Lectu) The Organic Chemistry of Drug Synthesis, Volume 3 (Organic Chemistry Series of Drug Synthesis) Advanced Digital Logic Design Using VHDL, State Machines, and Synthesis for FPGA's